ISL12022 RTC Accuracy Optimization Calibration Procedure

Introduction

Real Time Clock (RTC) devices contain an oscillator and normally require a crystal to operate with the required accuracy. Most common 32.768kHz crystal oscillators have a frequency tolerance of ±20ppm at +25°C, and a nonlinear temperature coefficient - Alpha - of -0.034ppm/°C^2. The temperature induced frequency drift is parabolic in nature, worsening as the crystal temperature deviates from the turnover temperature, referred to as the crystal's T0, which is commonly +25°C.

The following example illustrates the effects of frequency tolerance and Alpha on the accuracy of an RTC.

A crystal oscillator has a frequency error of -15ppm at +25°C and an Alpha of -0.034ppm/°C^2. At +40°C, the error becomes -22.7ppm (-15ppm + [-0.034ppm/°C^2*(40°C -25°C)^2]). A -22.7ppm drift means the RTC runs 22.7µs slower in a second, which seems very small at first glance, but accumulates to many minutes in a year. A -22.7ppm drift means losing 2 seconds in a day, 14 seconds in a week, 59 seconds in a month, and 716 seconds (11.9 minutes) in a year. A user of most common RTCs has to live with this error, but the ISL12022 RTC, with an embedded temperature compensation function, solves this problem. This application note describes a simple trimming procedure that optimizes the accuracy of an ISL12022 RTC, and presents calibrated and uncalibrated results for several crystals

Architecture of the ISL12022

The ISL12022 block diagram is shown in Figure 1. The "Temperature Sensor" and "Frequency Control" blocks are the essential components for compensating the effects of frequency tolerance and Alpha.

Temperature Sensor

The embedded temperature sensor produces an analog output voltage, that is input to an A/D converter to produce a 10-bit temperature value in degrees Kelvin. The temperature sensor measures the temperature immediately surrounding the ISL12022, including the nearby crystal, and the ISL12022 provides proper crystal compensation for the measured temperature.

Frequency Control

Frequency adjustment is controlled by five different registers:

- Initial ATR and DTR Trim Register (ITR0, address 0Bh)
- Beta Register (BETA, address 0Dh)
- ALPHA Cold Register (ALPHA, address 0Ch)
- ALPHA Hot Register (ALPHAH, address 2Dh)
- Crystal Turnover Temperature Register (XT0, address 2Ch)

The calibration procedure for trimming the five registers is discussed in the "ISL12022 Calibration Procedure" on page 2.

INITIAL ATR AND DTR TRIM REGISTER (ITR0)

This register trims the crystal's initial error (frequency tolerance at +25°C). Both digital (IDTR) and analog (IATR) trimming methods are available. Digital trimming uses clock pulse skipping and insertion for coarse frequency adjustment, while analog trimming adjusts internal load capacitors to pull the oscillator frequency off its nominal value. An adjustment range of +62.5ppm to -61.5ppm is possible with combined digital and analog trimming, where digital trimming provides ±30.5ppm via 2 bits, and analog trimming provides +32ppm to -31ppm of adjustment via 6 bits.

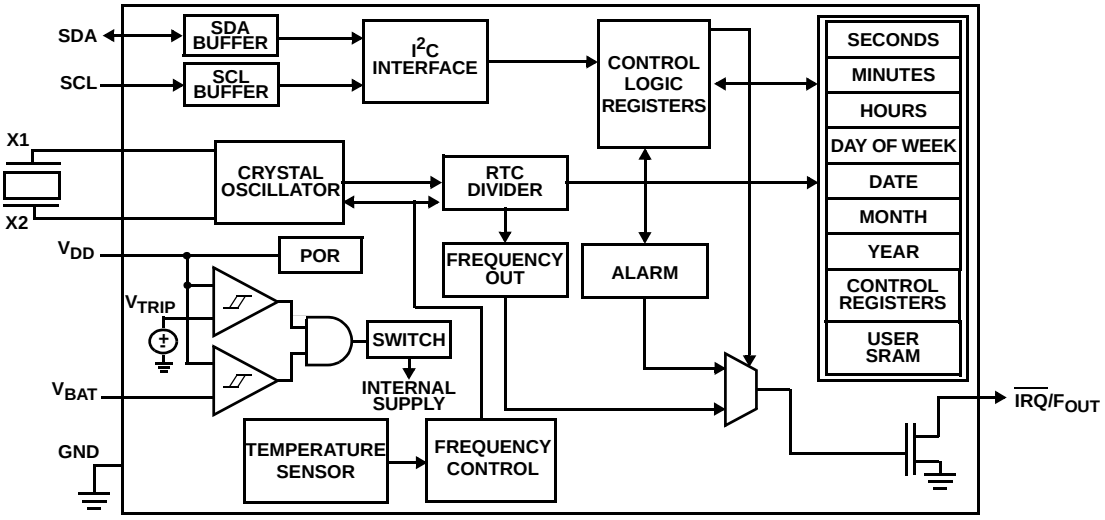

FIGURE 1. ISL12022 BLOCK DIAGRAM

BETA REGISTER (BETA)

Beta accounts for the Cm (motional capacitance) variation of crystals. Most crystals specify Cm around 2.2fF, which reduces the actual IATR steps from 1ppm/step to approximately 0.8ppm/step. Beta is then used to adjust for this variation, which restores the step size to 1ppm/step. The BETA register range is discontinuous, with allowed values ranging from 00000 to 01000 (00h to 08h) and from 10000 to 11111 (10h to 1Fh), as shown in Table 1.

ALPHA COLD REGISTER (ALPHA)

The ALPHA Cold Register, ALPHA, contains a 7-bit digital representation of the low temperature Alpha parameter (the crystal temperature coefficient). The ISL12022 uses this register value when the temperature is between -40°C and XT0 (typically +25°C). ALPHA <7:0> is the binary equivalent of: |The Crystal's Alpha Value| x 2048. For example, a crystal's typical Alpha of -0.034ppm/°C^2 is first scaled (|2048*(-0.034)| = 70d), and then converted to a binary number of 01000110b or hexadecimal value of 46h.

ALPHA HOT REGISTER (ALPHAH)

The ALPHA Hot Register, ALPHAH, contains a 7-bit digital representation of the high temperature Alpha parameter. The ISL12022 uses this register value when the temperature is between XT0 and +85°C. The ALPHAH register value is calculated in the same manner as previously described for the ALPHA register.

Separate Alpha registers are provided for the two temperature ranges in case a crystal has different temperature coefficients at high and low temperatures. Most crystal manufacturers specify only one Alpha value, and in this case ALPHA = ALPHAH.

CRYSTAL TURNOVER TEMPERATURE REGISTER (XT0)

The apex of the crystal's frequency drift vs. temperature curve occurs at a point called the turnover temperature, or XT0. Crystals normally have a turnover temperature between +20°C and +30°C, with most occurring near +25°C.

The ISL12022 allows setting the turnover temperature, such that temperature compensation can more exactly fit the crystal's curve. Table 2 shows the available XT0 values, which range from +17.5°C to +32.5°C in +0.5°C increments. The default value is 00000b or +25°C.

ISL12022 Calibration Procedure

The following sections detail the ISL12022 trimming procedure to determine the calibration values for the ITR0, BETA, XT0, ALPHA, and ALPHAH registers. Please use a high resolution frequency counter with at least 7 digits of resolution for frequency measurements. Before starting the procedure, completely power down (V_{DD} = V_{BAT} = 0V), and then power up the ISL12022 to ensure that all registers start at their default values.

Trimming Instructions (All tests at 25°C)

1. SELECT the $\overline{IRQ}/F_{OUT}$ OUTPUT FREQUENCY:
   Set INT register (ADDR = 08h) to any desired frequency (f) to be output on the $\overline{IRQ}/F_{OUT}$ pin, where f is the ideal frequency defined by the FO<3:0> bits. It is best to select 1Hz for the measurement for higher resolution. $\overline{IRQ}/F_{OUT}$ is an open-collector output, which requires a pull-up resistor to V_{DD}.
2. MEASURE f1 and CALCULATE fppm1:
   Set ITR0 register (address 0Bh) to 00h, then measure and record frequency f1 on $\overline{IRQ}/F_{OUT}$ pin. Calculate fppm1 using Equation 1:
   $$fppm1 = [(f1/f) - 1] \bullet 1E6 \quad \text{(EQ. 1)}$$
3. MEASURE f2 and CALCULATE fppm2:
   Set ITR0 register (address 0Bh) to 3Fh, then measure and record frequency f2 on $\overline{IRQ}/F_{OUT}$ pin. Calculate fppm2 using Equation 2:
   $$fppm2 = [(f2/f) - 1] \bullet 1E6 \quad \text{(EQ. 2)}$$
4. MEASURE f3 and CALCULATE fppm3:
   Set ITR0 register (address 0Bh) to 20h, then measure and record frequency f3 on $\overline{IRQ}/F_{OUT}$ pin. Calculate fppm3 using Equation 3:
   $$fppm3 = [(f3/f) - 1] \bullet 1E6 \quad \text{(EQ. 3)}$$
5. CALCULATE AT Step Size (ATSS):
   Calculate the ATSS using Equation 4:
   $$ATSS = |(fppm1 - fppm2)|/63 \quad \text{(EQ. 4)}$$
   where fppm1 is from Equation 1 and fppm2 is from Equation 2.
6. TRIM BETA:
   Using the calculated ATSS from Equation 4, find the closest value in the "AT STEP SIZE" column in the "BETA Look-up Table" (Table 1) and set the BETA register (address 0Dh) to the corresponding BETA code from the first column.
   BETA TRIMMED.
7. TRIM IDTR0 and IATR0 (ITR0 register [address 08h])

   A. Check if digital trim (DT) is required. If (fppm3 > 31ppm) then set IDTR0 <1:0> to 11b and the new fppm3 = fppm3 - 30.5ppm. If (fppm3 < -32ppm) then set IDTR0 <1:0> to 01b and the new fppm3 = fppm3 + 30.5ppm. If DT is not required, set IDTR0 <1:0> to 00b.
   IDTR0 TRIMMED

   B. If DT was required per Step A, use the newly calculated fppm3 from Step A for the following calculation of the IATR0 code. If DT was not required, use the original fppm3 from Equation 3. Calculate the required analog trim adjustment (DeltaAT) using Equation 5:
   $$DeltaAT = |fppm3|/ATSST \quad \text{(EQ. 5)}$$
   where ATSST is the selected Table 1 ATSS value from Instruction 6. DeltaAT must be a positive number, and is rounded to the nearest integer value.

   C. Calculate the required analog trim (AT) value using Equation 6:
   $$\text{If } (fppm3 < 0)\ AT = 32 - DeltaAT \text{ else } AT = 32 + DeltaAT \quad \text{(EQ. 6)}$$
   Set IATR0<5:0> to the binary equivalent of AT.
   IATR0 TRIMMED.

TABLE 1. BETA LOOK-UP TABLE

BETA<4:0> CODE	AT STEP SIZE
01000	0.5000
00111	0.5625
00110	0.6250
00101	0.6875
00100	0.7500
00011	0.8125
00010	0.8750
00001	0.9375
00000	1.0000
10000	1.0625
10001	1.1250
10010	1.1875
10011	1.2500
10100	1.3125
10101	1.3750
10110	1.4375
10111	1.5000
11000	1.5625
11001	1.6250
11010	1.6875
11011	1.7500
11100	1.8125
11101	1.8750
11110	1.9375
11111	2.0000

8. TRIM XT0:
   Please refer to the crystal's data sheet for the XT0 or turnover temperature value; the typical value will suffice. Use the "XT0 Look-up Table" (Table 2) to find the corresponding XT0 code. Set the XT0 register (address 2Ch) to the XT0 code.
   XT0 TRIMMED.
9. TRIM ALPHA and ALPHAH:
   Please refer to the crystal's data sheet for Alpha (crystal temperature coefficient). Alpha is expressed in units of ppm/°C^2; the typical value will suffice.
   Scale Alpha using Equation 7:

$$\text{Scaled Alpha} = (|\text{Actual Alpha Value in ppm}| \times 2048) \quad \text{(EQ. 7)}$$

   Round Scaled Alpha to the nearest integer and convert the result to a binary number. Set the ALPHA register (address 0Ch) and the ALPHAH register (address 2Dh) to the Scaled Alpha binary value.
   ALPHA and ALPHAH TRIMMED.

TABLE 2. XT0 LOOK-UP TABLE

XT<4:0> CODE	TURNOVER TEMPERATURE
01111	32.5
01110	32.0
01101	31.5
01100	31
01011	30.5
01010	30
01001	29.5
01000	29.0
00111	28.5
00110	28.0
00101	27.5
00100	27.0
00011	26.5
00010	26.0
00001	25.5
00000	25.0
10000	25.0
10001	24.5
10010	24.0
10011	23.5
10100	23.0
10101	22.5
10110	22.0
10111	21.5
11000	21.0
11001	20.5
11010	20.0
11011	19.5
11100	19.0
11101	18.5
11110	18.0
11111	17.5

Trimming Example

The following is an example of the trimming procedure actually preformed in the lab with the ISL12022.

This example uses the Citizen CM200C 32.768kHz 12.5pF crystal. The crystal has a typical frequency tolerance of ±20ppm, a typical turnover temperature of +25°C ± 5°C, and a typical temperature coefficient of -0.034ppm/°C^2.
(Note: Cycle V_{DD} and V_{BAT} to reset all registers to default).

1. SELECT $\overline{IRQ}/F_{OUT}$ OUTPUT FREQUENCY:
   $\overline{IRQ}/F_{OUT}$ is connected to a 2kΩ pull-up resistor to V_{DD}. FO bits in INT Register (address = 08h) are set to 0011b (X3h) to select a 1024Hz frequency for the measurements.

2. MEASURE f1 and CALCULATE fppm1 using Equation 8:
   Set ITR0 register (address 0Bh) to 00h; f1 is 1024.0095Hz from the measurement at the $\overline{IRQ}/F_{OUT}$ pin.

   $$fppm1 = [(1024.0095/1024) - 1] \bullet 1E6 = 9.3ppm \quad \text{(EQ. 8)}$$

3. MEASURE f2 and CALCULATE fppm2 using Equation 9:
   Set ITR0 register (address 0Bh) to 3Fh; f2 is 1023.9351Hz from the measurement at the $\overline{IRQ}/F_{OUT}$ pin.

   $$fppm2 = [(1023.9351/1024) - 1] \bullet 1E6 = -63.4ppm \quad \text{(EQ. 9)}$$

4. MEASURE f3 and CALCULATE fppm3 using Equation 10:
   Set ITR0 register (address 0Bh) to 20h; f3 is 1023.9713Hz from the measurement at the $\overline{IRQ}/F_{OUT}$ pin.

   $$fppm3 = [(1023.9713/1024) - 1] \bullet 1E6 = -28ppm \quad \text{(EQ. 10)}$$

5. CALCULATE ATSS using Equation 11:

   fppm1 = 9.3ppm, fppm2 = -63.4ppm

   $$ATSS = |(9.3 - (-63.4))|/63 = 1.154 \quad \text{(EQ. 11)}$$

6. TRIM BETA:
   ATSS = 1.154; the closest ATSS from the "BETA Look-up Table" (Table 1) is 1.125. The corresponding BETA code for ATSS of 1.125 is 10001b or 11h.
   Set the BETA register (address 0Dh) to 10001b (11h).
   BETA TRIMMED.

7. TRIM IDTR0 and IATR0:

   A. Check if DT is required using Equation 12:

   $$fppm3 = -28ppm$$
   $$Is\ (fppm3 > 32)NO \quad \text{(EQ. 12)}$$
   $$Is\ (fppm3 < -31)NO$$

   Both answers are "NO", so DT is not required; set IDTR0<1:0> to 00b

   B. Since DT is not required, use the original fppm3 from Step 4, and the ATSS value picked from the BETA look-up table in Step 6.
   Calculate trimmed code for IATR (DeltaAT) using Equation 13, and round to the closest integer:

   fppm3 = -28ppm, ATSST = 1.125

   $$DeltaAT = |-28|/1.125 = 24.9 = 25 \quad \text{(EQ. 13)}$$

   C. Find IATR code (AT) using Equation 14:

   $$fppm3 = -28ppm$$
   $$Since\ (fppm3 < 0) \quad \text{(EQ. 14)}$$
   $$AT = 32 - 25 = 7\text{, so IATR0<5:0> = 000111b}$$

   D. IDTR0<1:0> = 00b, IATR0 <5:0> = 000111b
   Set ITR0 register (address 0Bh) to 00000111b (07h).
   IDTR0 and IATR0 TRIMMED.

8. TRIM XT0:
   From the CM200C data sheet, the typical XT0 is +25°C, and from the "XT0 Look-up Table" (Table 2), XT0 of +25°C corresponds to 00000b or 10000b. Code 00000b is selected to be the XT0 code.
   Set XT0 register (address 2Ch) to 00000b (00h).
   XT0 TRIMMED.

9. TRIM ALPHA and ALPHAH:
   From the CM200C data sheet, the typical Alpha is -0.034ppm/°C^2.

   $$Scaled\ Alpha = (|-0.034| \times 2048) = 69.6 = 70 = 1000110b \quad \text{(EQ. 15)}$$

   Set ALPHA register (address 0Ch) and ALPHAH register (address 2Dh) to 1000110b (46h).
   ALPHA and ALPHAH TRIMMED.

10. Set the TSE bit (and BTSE and BTSR if desired) in the Beta register (address 0Dh) to enable temperature measurement and compensation. The frequency error should now measure close to 0ppm.

Compensated and Uncompensated Test Results with Different Crystals

Three different 32.768kHz, 12.5pF crystals were tested to demonstrate the improvement achieved by performing the calibration procedure. The three crystals are a Citizen CM200C, an Epson MC-156, and an Abracon AB26T. The CM200C and MC-156 are surface mount crystals with an operational range of -40°C to +85°C. AB26T is a cylinder type crystal, with an operational range of -20°C to +70°C.

The measurements were made with V_{DD} = 3.3V, over temperature, and used three compensation settings:

1. No crystal temperature compensation;
2. Temperature compensation with default factory data;
3. Temperature compensation with calibrated data for the actual RTC crystal.

"No crystal temperature compensation" means that the ISL12022's temperature compensation function was disabled during testing. To disable the function, simply write the TSE bit (Temperature Sensor Enabled, bit 7 at address 0Dh) to 0. These uncompensated measurement results illustrate the parabolic temperature behavior of the crystal and the typical performance of an ordinary RTC.

"Temperature compensated with default factory data" means that the ISL12022 performs temperature compensation with pre-programmed (factory set) ITR0, BETA, ALPHA, ALPHAH, and XT0 values. The values are set for a crystal with 0ppm frequency tolerance (i.e., defaults can't compensate for tolerance, since it may positive or negative), 2.2fF motional capacitance, -0.034ppm/°C^2 Alpha, and +25°C turnover temperature. The measurement results for the ISL12022 using these typical crystal parameters for temperature compensation, illustrate the advantage of using the ISL12022 over an ordinary RTC.

"Temperature compensation with calibrated data" means that the ISL12022 performs temperature compensation with calibrated ITR0, BETA, ALPHA, ALPHAH, and XT0 values, derived from the procedure described in this Application Note. After temperature compensating with calibrated data, the test results show the advantage of the calibrated ISL12022 versus the uncalibrated ISL12022.

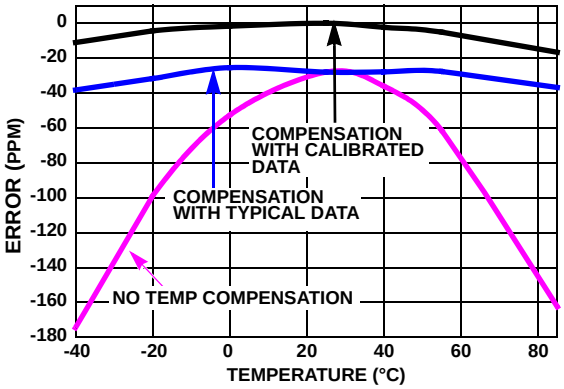

FIGURE 2. CITIZEN CM200C ERROR vs TEMPERATURE (-40 °C TO +85 °C)

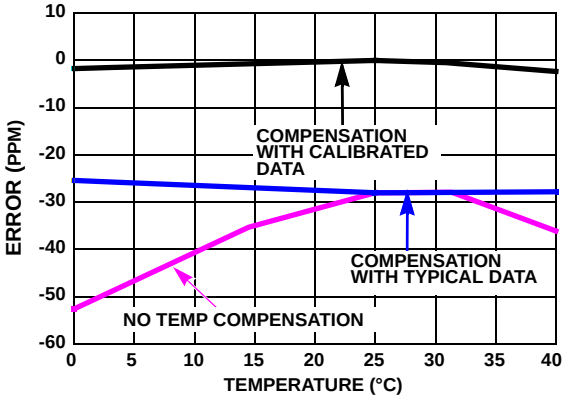

FIGURE 3. CITIZEN CM200C ERROR vs TEMPERATURE (0 °C TO +40 °C)

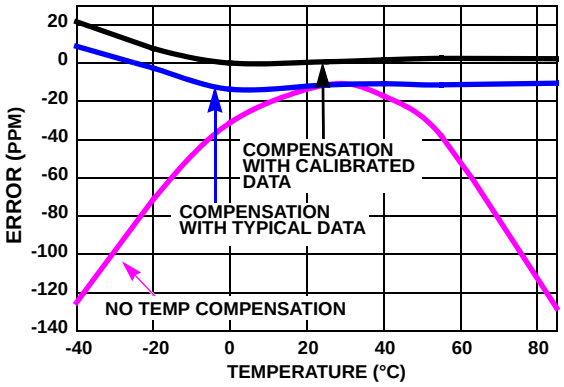

FIGURE 4. EPSON MC-156 ERROR vs TEMPERATURE (-40 °C TO +85 °C)

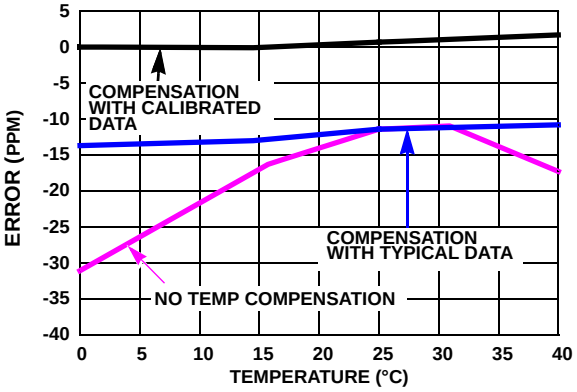

FIGURE 5. EPSON MC-156 ERROR vs TEMPERATURE (0 °C TO 40 °C)

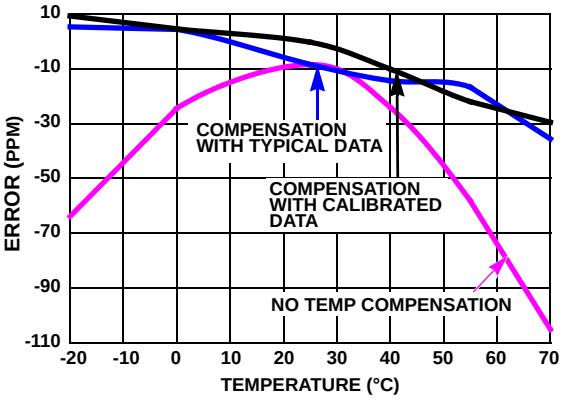

FIGURE 6. ABRACON AB26T ERROR vs TEMPERATURE (-20 °C TO +70 °C)

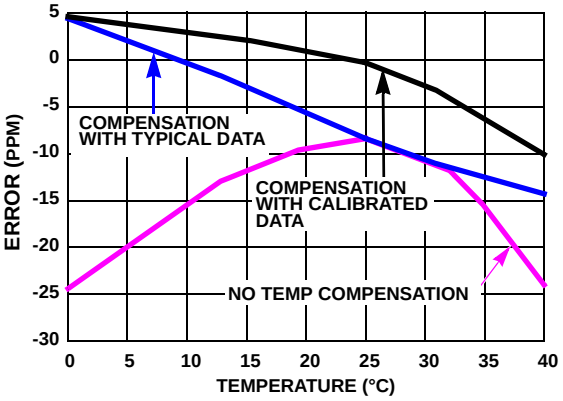

FIGURE 7. ABRACON AB26T ERROR vs TEMPERATURE (0 °C TO +40 °C)

As clearly shown in all the “Error vs Temperature” graphs, a high accuracy RTC system - with only ±10ppm error from 0°C to +40°C or ±20ppm error from -40°C to +85°C - is achievable by using the ISL12022’s embedded temperature compensation function with a simple calibration procedure.

Layout Considerations

The ISL12022’s crystal input pin (X1) has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit avoids noise pickup and insures accurate clocking.

Figure 8 shows a suggested layout for the ISL12022 RTC using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines, or any high speed logic lines, in the vicinity of the crystal. These logic signals can induce noise in the oscillator circuit, causing misclocking.
2. Add a ground trace around the crystal with one end connected to the ISL12022 ground. This provides a termination point for emitted noise in the vicinity of the RTC device.

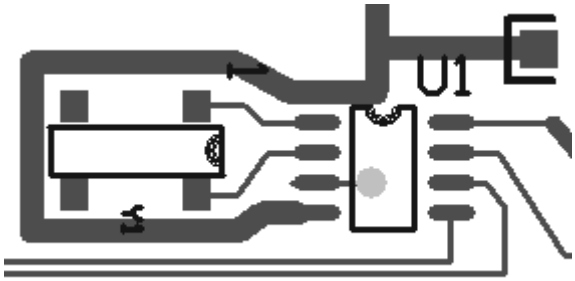

FIGURE 8. SUGGESTED LAYOUT FOR ISL12022 AND CRYSTAL

In addition, it is a good idea to avoid any ground or power planes under the X1 and X2 pins and traces, and under the crystal’s body. Any nearby plane affects the crystal’s load capacitance, and therefore the oscillator accuracy. If the $\overline{IRQ}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{DD} pins can be treated as a ground, and should be routed around the crystal.

Conclusion

The ISL12022 helps an RTC system achieve higher accuracy after a simple calibration procedure. However, the user programmed compensation values are lost once the RTC’s V_{DD} and V_{BAT} are completely powered down. In order to restore the compensation data, the system has to store the data somewhere - such as an EEPROM or flash memory in the system - and then write the data back into the ISL12022 after it powers up again. Alternatively, if ±30-40ppm, full temperature timing errors are tolerable, using the ISL12022’s default compensation settings eliminates the data storage requirement. The default compensation settings are stored in on-chip EEPROM, and are restored to the compensation registers after every total power failure.

In order for the ISL12022 to achieve an extremely high accuracy of ±3.5ppm or better from -40°C to +85°C, the user has to obtain an XT0 accurate to ±0.5°C and an Alpha value accurate to ±0.0003ppm/°C^2 which is ±1% of the typical value from the crystal manufacturer. This requires testing at a minimum of three temperature points, and then performing a set of calculations to determine the precise XT0 and Alpha parameters. These tests could be time consuming, so the extra accuracy gained may not be worth the additional time.

To circumvent the ISL12022’s calibration requirement, Intersil has added the ISL12020M and ISL12022M to our RTC portfolio. The “M” stands for module, where the crystal and the ISL12022 die are integrated into one package. Both module versions are factory calibrated for the full -40°C to +85°C temperature range, so no user characterization is required. All the calibration/compensation data is stored in on-chip, nonvolatile memory, so the ISL1202XM retain their settings when the RTCs are unpowered. The ISL12020M is packaged in a 20 “lead” 4mm x 5.5mm DFN, and is the world’s smallest RTC module package with ±5ppm or better accuracy from -40°C to +85°C. The ISL12022M is a 20 lead SOIC version, for applications requiring a leaded package.

The ISL12020M and ISL12022M RTC modules with embedded crystals and factory calibrated temperature compensation, are the best solutions for systems requiring ±5ppm or better accuracy from -40°C to +85°C. Please contact your local sales representative if better than ±5ppm accuracy is required.

If your system requires accuracy of only ±10ppm from 0°C to +40°C, or ±20ppm from -40°C to +85°C, then the ISL12022 RTC is a very good solution, if one follows the ISL12022 calibration procedure previously described.